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<u>L11</u>	l3 and l6	24	<u>L11</u>
<u>L10</u>	l3 and l5	52	<u>L10</u>
<u>L9</u>	(712/33)[CCLS]	131	<u>L9</u>
<u>L8</u>	(710/310,132,314)[CCLS]	621	<u>L8</u>
<u>L7</u>	(710/305-314)![CCLS]	3771	<u>L7</u>
<u>L6</u>	(712/29-38, 225, 229)[CCLS]	1641	<u>L6</u>
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<u>L2</u>	L1 near45 (cpu or central near1 processing near1 unit)	8	<u>L2</u>
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IEEE JNL	IEEE Journal or Magazine
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IEEE CNF	IEEE Conference Proceeding
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Citation & Abstract

[view selected items](#)[Select All](#) [Deselect All](#)**1. FPGA implemented fast two's complement serial-parallel multiplier with PCI interface**

Khalil, A.H.; Ashour, M.A.; Salama, A.E.; Saleh, H.I.;
[Microelectronics, 1998, ICM '98, Proceedings of the Tenth International Conference on](#)
 14-16 Dec. 1998 Page(s):21 - 24
 Digital Object Identifier 10.1109/ICM.1998.825558

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**2. A flexible compatible PCI interface for nuclear experiments**

Saleh, H.; Engels, R.; Reinartz, R.; Reinhart, P.; Rongen, F.;
[Nuclear Science Symposium, 1997, IEEE](#)
 9-15 Nov. 1997 Page(s):704 - 706 vol.1
 Digital Object Identifier 10.1109/NSSMIC.1997.672678

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**3. A flexible compatible PCI interface for nuclear experiments**

Saleh, H.; Engels, R.; Reinartz, R.; Reinhart, P.; Rongen, F.;
[Nuclear Science, IEEE Transactions on](#)
 Volume 45, Issue 3, Part 1, June 1998 Page(s):849 - 851
 Digital Object Identifier 10.1109/23.682649

[AbstractPlus](#) | Full Text: [PDF](#)(280 KB) IEEE JNL
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**4. Single chip PCI bridge and memory controller for PowerPC microprocessors**

Garcia, M.J.; Reynolds, B.K.;
[Computer Design: VLSI in Computers and Processors, 1994, ICCD '94, Proceedings, IEEE Intern](#)
 10-12 Oct. 1994 Page(s):409 - 412
 Digital Object Identifier 10.1109/ICCD.1994.331938

[AbstractPlus](#) | Full Text: [PDF](#)(388 KB) IEEE CNF
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Nishi, H.; Tasho, K.; Yamamoto, J.; Kudoh, T.; Amano, H.;
[High-Performance Distributed Computing, 2000, Proceedings, The Ninth International Symposium](#)
 1-4 Aug. 2000 Page(s):296 - 297
 Digital Object Identifier 10.1109/HPDC.2000.868665

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 Fanti, V.; Marzeddu, R.; Randaccio, P.;
[Nuclear Science Symposium Conference Record, 2002 IEEE](#)
 Volume 2, 10-16 Nov. 2002 Page(s):944 - 946 vol.2
 Digital Object Identifier 10.1109/NSSMIC.2002.1239479
[AbstractPlus](#) | Full Text: [PDE\(1793 KB\)](#) | [IEEE CNF](#)
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 Wei, R.; Gao, X.H.; Jin, M.H.; Liu, Y.W.; Liu, H.; Seitz, N.; Gruber, R.; Hirzinger, G.;
[Intelligent Robots and Systems, 2005 \(IROS 2005\), 2005 IEEE/RSJ International Conference on](#)
 2-6 Aug. 2005 Page(s):523 - 528
 Digital Object Identifier 10.1109/IROS.2005.1545469
[AbstractPlus](#) | Full Text: [PDE\(504 KB\)](#) | [IEEE CNF](#)
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- ☐ **8. Single-chip FPGA Implementation of a cryptographic co-processor**
 Crowe, F.; Daly, A.; Kerins, T.; Marnane, W.;
[Field-Programmable Technology, 2004. Proceedings, 2004 IEEE International Conference on](#)
 2004 Page(s):279 - 285
 Digital Object Identifier 10.1109/FPT.2004.1393279
[AbstractPlus](#) | Full Text: [PDE\(731 KB\)](#) | [IEEE CNF](#)
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 Krishnamurthy, R.; Yalamanchill, S.; Schwan, K.; West, R.;
[High Performance Interconnects, 2002. Proceedings, 10th Symposium on](#)
 21-23 Aug. 2002 Page(s):52 - 61
 Digital Object Identifier 10.1109/CONECT.2002.1039257
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 Santhanam, S.; Allmon, R.; Anne, K.; Blake, R.; Bunker, N.; Campbell, B.; Carlson, M.; Zongjian Cl
 Do; Dobberpuhl, D.; Ingino, J.; Kidd, D.; Kruckemyer, D.; Jong Lee; Murray, D.; Nishimoto, S.; O'Do
 Panich, M.; Pearce, M.; Priore, D.; Rodriguez, D.; Rogenmoser, R.; Dongwook Suh; Sundaresan, V
 Kaenel, V.; Yee, G.; Yiu, G.; Vo, C.; Wen, R.;
[VLSI Circuits, 2001. Digest of Technical Papers, 2001 Symposium on](#)
 14-16 June 2001 Page(s):107 - 110
 Digital Object Identifier 10.1109/VLSIC.2001.934209
[AbstractPlus](#) | Full Text: [PDE\(300 KB\)](#) | [IEEE CNF](#)
[Rights and Permissions](#)
- ☐ **11. Silicon single-chip television tuner technology**
 Birlson, S.; Esquivel, J.; Nelsen, P.; Norsworthy, J.; Richter, K.;
[Consumer Electronics, 2000. ICCE, 2000 Digest of Technical Papers, International Conference on](#)
 13-15 June 2000 Page(s):38 - 39
 Digital Object Identifier 10.1109/ICCE.2000.854486
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- ☐ **12. Integration of large-scale FPGA and DRAM in a package using chip-on-chip technology**
 Wang, M.X.; Suzuki, K.; Dai, W.W.-M.; Low, Y.L.; O'Conner, K.J.; Tai, K.L.;
[Design Automation Conference, 2000. Proceedings of the ASP-DAC 2000, Asia and South Pacific](#)
 25-28 Jan. 2000 Page(s):205 - 210
 Digital Object Identifier 10.1109/ASPDAC.2000.835097

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13. Design and Implementation of a high-speed ATM host interface controller

Chan Kim; Jong-Arm Jun; Yeong-Ho Park; Kyu-Ho Lee; Hyup-Jong Kim;
[Information Networking, 1998. \(ICOIN-12\) Proceedings. Twelfth International Conference on](#)
21-23 Jan. 1998 Page(s):525 - 528

Digital Object Identifier 10.1109/ICOIN.1998.648440

[AbstractPlus](#) | Full Text: [PDF](#)(44 KB) [IEEE CNF](#)
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14. High speed neural network chip for trigger purposes in high energy physics

Eppler, W.; Fischer, T.; Gemmeke, H.; Menchikov, A.;
[Design, Automation and Test in Europe, 1998. Proceedings](#)
23-26 Feb. 1998 Page(s):108 - 115

Digital Object Identifier 10.1109/DATE.1998.655844

[AbstractPlus](#) | Full Text: [PDF](#)(84 KB) [IEEE CNF](#)
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15. FX1000: a high performance single chip Gigabit Ethernet NIC

Ross, M.; Bechtolsheim, A.; Le, M.T.; O'Sullivan, J.;
[Compton '97. Proceedings. IEEE](#)

23-26 Feb. 1997 Page(s):218 - 223

Digital Object Identifier 10.1109/CMPCON.1997.584711

[AbstractPlus](#) | Full Text: [PDF](#)(332 KB) [IEEE CNF](#)
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16. Neural network chips for trigger purposes in high energy physics

Gemmeke, H.; Eppler, W.; Fischer, T.; Menchikov, A.; Neusser, S.;
[Nuclear Science Symposium, 1996. Conference Record, 1996 IEEE](#)
Volume 1, 2-9 Nov. 1996 Page(s):302 - 306 vol.1

Digital Object Identifier 10.1109/NSSMIC.1996.590964

[AbstractPlus](#) | Full Text: [PDF](#)(496 KB) [IEEE CNF](#)
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17. Designing a PC with the DECchip 21066

Sanders, D.;
[Compton Spring '94. Digest of Papers.](#)

28 Feb.-4 March 1994 Page(s):414 - 417

Digital Object Identifier 10.1109/CMPCON.1994.282891

[AbstractPlus](#) | Full Text: [PDF](#)(292 KB) [IEEE CNF](#)
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18. A 7.1-GB/s low-power rendering engine in 2-D array-embedded memory logic CMOS for port system

Yong-Ha Park; Seon-Ho Han; Jung-Hwan Lee; Hoi-Jun Yoo;
[Solid-State Circuits, IEEE Journal of](#)

Volume 36, Issue 6, June 2001 Page(s):944 - 955

Digital Object Identifier 10.1109/4.924857

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19. Metal Fix and Power Network Repair for SOC

Qing K. Zhu; Kolze, P.;
[Emerging VLSI Technologies and Architectures, 2006. IEEE Computer Society Annual Symposium](#)
Volume 00, 02-03 March 2006 Page(s):33 - 37

Digital Object Identifier 10.1109/ISVLSI.2006.61

[AbstractPlus](#) | Full Text: [PDF](#)(200 KB) [IEEE CNF](#)
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- ☐ **20. A programmable processor with 4096 processing units for media applications**
 Krikelis, A.; Jalowiecki, I.P.; Bean, D.; Bishop, R.; Facey, M.; Boughton, D.; Murphy, S.; Whitaker, P.
Acoustics, Speech, and Signal Processing, 2001. Proceedings. (ICASSP '01). 2001 IEEE International Conference on
 Volume 2, 7-11 May 2001 Page(s):937 - 940 vol.2
 Digital Object Identifier 10.1109/ICASSP.2001.941070
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 Mair, H.; Liming Xiu;
Solid-State and Integrated Circuit Technology, 1998. Proceedings. 1998 5th International Conference on
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 Digital Object Identifier 10.1109/ICSICT.1998.785894
[AbstractPlus](#) | Full Text: [PDF](#)(284 KB) [IEEE CNF](#)
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- ☐ **22. Reconfigurable computing at Xilinx**
 Guccione, S.A.;
Digital Systems Design, 2001. Proceedings. Euromicro Symposium on
 4-6 Sept. 2001 Page(s):102
 Digital Object Identifier 10.1109/DSD.2001.952124
[AbstractPlus](#) | Full Text: [PDF](#)(35 KB) [IEEE CNF](#)
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- ☐ **23. Dynamic space processor architecture built on commercial open system interface standard**
 Marshall, J.R.;
Digital Avionics Systems Conference, 1999. Proceedings. 18th
 Volume 2, 24-29 Oct. 1999 Page(s):9.B.2-1 - 9.B.2-8 vol.2
 Digital Object Identifier 10.1109/DASC.1999.863667
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